Product Information

DIVA Automation

Innovation in Motion

DA2000

Quadrature Encoder Decoder

Original release, September 22, 2007

Description

The DA2000, Quadrature Encoder Decoder converts a standard two-channel incremental encoder signal into pulses to control an external up/down counter.

By counting these pulses, a representation of the position of the encoder can be maintained to a dynamic range determined by the number of stages of the counter circuit.

Version A supports only single-ended encoder signals. Later versions support differential inputs with phase inversion capability and support for index pulses.

- High speed--up to 20 MHz
- Easy to use
- Unlimited dynamic range (Using external counters.)
- Low power
- Through-hole and surface mount packages
- Commercial and industrial temperature ranges
- TTL level I/O

Application

Quadrature encoders utilize a count sequence known as a "Grey code". This sequence is chosen for two reasons: It is a more reliable code sequence than binary code because only one bit is allowed to change for each change of state. This condition is met by simply providing two identical channels that are offset by 90^0. This quarter-cycle offset between channels is described as being in quadrature.

To adapt the Grey code to a binary system, it is necessary to decode the Grey code to determine the direction of the sequence. The DA2000 performs this decoding function and provides signals to control an external up/down counter, such as the 74LS193, a generic 4-bit up/down counter. DIVA also offers a companion 8-bit up/down counter at slightly higher cost than the TTL counter. (DA2010)

Because of the 90^0 offset between signals, the two channels exhibit a four-step sequence each cycle. This characteristic provides four count pulses for each cycle of the encoder as well as the information necessary to decode positive and negative motion of the encoder.

A 500-line encoder will therefore produce 2000 count pulses per rotation.

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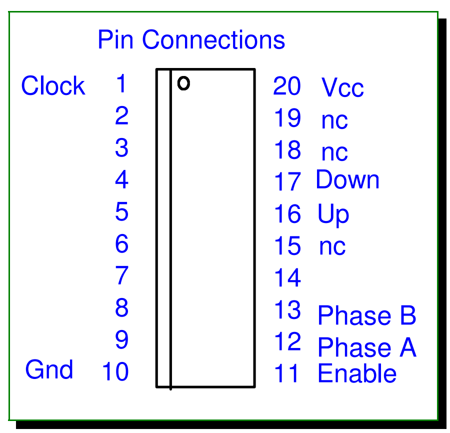
The clock frequency determines the maximum encoder input rate. The clock is used to synchronize the input signals to prevent false outputs and to standardize the output pulses to the width of one clock cycle. A 1 MHz clock will produce output pulses with a width of 1 microsecond, for example, regardless of the encoder input rate.

Therefore, the clock rate should be set to at least twice the highest expected encoder frequency.

However, the highest frequency to be expected is not determined by the maximum velocity, but by vibration-induced pulses when the encoder is at rest near a transition between two states. In practice, it is best to use the highest clock frequency which can be reliably counted by the external counter. For most applications, 10 MHz is a good selection.



Top view of DIP package. Note: Do not connect to pins marked nc.

DIVA Automation
sales@divaauto.com
+1-800-984-DIVA

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